



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,144	08/27/2004	Douglas D. Coolbaugh	BUR920040107US1	5143
45601 7590 01/21/2009 SCULLY, SCOTT, MURPHY & PRESSER, P.C. 400 GARDEN CITY PLAZA Suite 300 GARDEN CITY, NY 11530				
EXAMINER				
NGUYEN, KHIEM D				
ART UNIT		PAPER NUMBER		
2823				
MAIL DATE		DELIVERY MODE		
01/21/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/711,144

Applicant(s)

COOLBAUGH ET AL.

Examiner

KHIEM D. NGUYEN

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 December 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 6-9 and 12-20 is/are pending in the application.
- 4a) Of the above claim(s) 15-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-9 and 12-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/S508)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on August 25th, 2008 has been entered. Claims 1-3, 6-9 and 12-20 are pending in this application in which claims 15-20 have been withdrawn from consideration.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
3. Claims 1-3, 6-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coolbaugh et al. (U.S. Pub. 2003/0122128) in view of Chen et al. (U.S. Pub. 2004/0114288).

In re claim 1, Coolbaugh discloses a varactor structure comprising: a semiconductor substrate **10** of a first conductivity type including a subcollector **12** of a second conductivity type (see page 2, paragraph [0038]) located below an upper region of the semiconductor substrate **10**, the first conductivity type is

different from the second conductivity type; a well region located in the upper region of the semiconductor substrate **10**, wherein the well region includes outer well regions **22** of the second conductivity type and an inner well region **18** of the first conductivity type, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **16** (see page 2, paragraph [0037] to page 3 paragraph [0043] and FIGS. 1-5) and each outer well region **22** has an upper surface which includes a source/drain region (see page 3, paragraph [0043]); and

a field effect transistor having at least a gate conductor **54** of the first conductivity type located above the inner well region **18** (see page 3, paragraph [0047] to page 4, paragraph [0050] and FIGS. 6-10); and

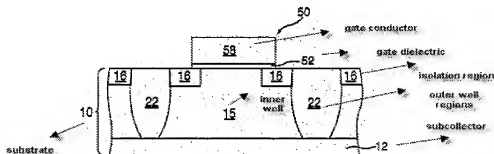


FIG. 10

wherein, the outer well regions **22** and the inner well region **18** are in contact with the subcollector **12** having the second conductivity type (see page 3, paragraph [0043]), wherein said each well of alternating conductivity type of said well region extends beneath the isolation region to the subcollector **12** such that neighboring well regions **18**, **22** are in contact with each other along an entire depth of each well region, wherein the subcollector **12** continuously extends

through the outer well region **22** and the inner well region **18** of the semiconductor substrate (see FIGS. 5 and 10 and related text).

However, **Coolbaugh** does not specifically disclose a semiconductor layer of a first conductivity type beneath the subcollector.

Chen disclose a semiconductor structure comprising a semiconductor substrate including a subcollector **34** of a second conductivity type (N-type) located below an upper region of the semiconductor substrate and a semiconductor layer **30** of a first conductivity type (P-type) beneath the subcollector **34**, a well region located in the upper region of the semiconductor substrate, wherein the well region includes outer well region **36** of second conductivity type and an inner well region **38** of the first conductivity type, and a field effect transistor having at least a gate conductor **42** located above the inner well region 38 (see Page 2, paragraph [0020] and FIG. 4B).

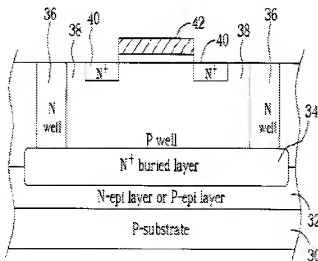


Fig. 4B

As Chen disclosed, one of ordinary skill in the art would have been motivated to provide a semiconductor layer of a first conductivity type beneath the subcollector in order for the N-epi layer to be formed thereon so that the subcollector can be embedded in the N-epi layer (see Page 2, paragraph [0020] of Chen).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Coolbaugh reference with the semiconductor layer of a first conductivity type formed beneath the subcollector as taught by Chen in order for the N-epi layer to be formed thereon so that the subcollector can be embedded in the N-epi layer (see Page 2, paragraph [0020] of Chen).

In re claim 2, as applied to claim 1 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the first conductivity type comprises a p-type dopant and second conductivity type comprises a n-type dopant (see page 2, paragraphs [0038]-[0041] of Coolbaugh).

In re claim 3, as applied to claim 1 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the first conductivity type comprises a n-type dopant and the second conductivity type comprises a p-type dopant (see page 2, paragraphs [0038]-[0041] of Coolbaugh).

In re claim 6, as applied to claim 1 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the upper region of the semiconductor substrate 10 comprises an epitaxial semiconductor

layer (optional epi Si layer, not shown) (see page 2, paragraph [0039] of Coolbaugh).

In re claim 7, as applied to claim 1 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the field effect transistor further comprises a gate dielectric **52** located beneath the gate conductor **54**, a hard mask **56** located on the gate conductor **54**, at least one spacer located on sidewalls of the gate conductor **54** and abutting source/drain regions (see page 3, paragraph [0059] to page 4, paragraph [0050] and FIG. 9 of Coolbaugh).

In re claim 8, as applied to claim 1 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the gate conductor **54** comprises polysilicon (see page 3, paragraph [0049] of Coolbaugh).

In re claim 9, Coolbaugh discloses a varactor structure comprising a p-type semiconductor substrate **10** including an n-type subcollector **12** located below an upper region (see page 2, paragraph [0038]) of the semiconductor substrate **10**; a well region located in the upper region of the semiconductor substrate **10**, wherein the well region includes outer N-well regions **22** and an inner P-well region **18**, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **16** (see page 2, paragraph [0037] to page 3, paragraph [0043] and FIGS. 1-5) and each outer well region **22** has an upper surface which includes a source/drain region (see

page 3, paragraph [0043]); and a field effect transistor having at least a p-type gate conductor **54** located above the inner P-well region **18**, the outer N-well regions **22** and the inner P-well region **18** are in contact with the n-type subcollector **12** (see page 3, paragraph [0047] to page 4, paragraph [0050] and FIGS. 6-10),

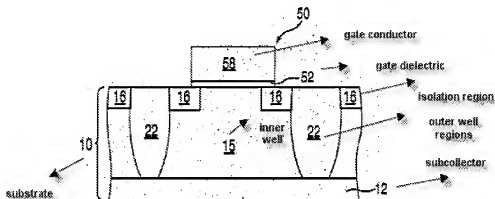


FIG. 10

wherein the outer N-well regions **22** and the inner P-well region **18** extend beneath the isolation region **16** to the n-type subcollector such that neighboring well regions **18**, **22** are in contact with each other along an entire depth of each well region, wherein the n-type subcollector **12** continuously extends through the outer N-well regions **22** and the inner P-well region **18** (see FIGS. 5 and 10 and related text).

However, Coolbaugh does not specifically disclose a p-type semiconductor layer beneath the n-type subcollector.

Chen disclose a semiconductor structure comprising a semiconductor substrate including a subcollector **34** of a second conductivity type (N-type)

located below an upper region of the semiconductor substrate and a semiconductor layer **30** of a first conductivity type (P-type) beneath the n-type subcollector **34**, a well region located in the upper region of the semiconductor substrate, wherein the well region includes outer well region **36** of second conductivity type and an inner well region **38** of the first conductivity type, and a field effect transistor having at least a gate conductor **42** located above the inner well region **38** (see Page 2, paragraph [0020] and FIG. 4B).

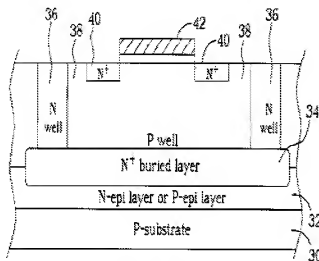


Fig. 4B

As Chen disclosed, one of ordinary skill in the art would have been motivated to provide a p-type semiconductor layer beneath the n-type subcollector in order for the N-epi layer to be formed thereon so that the n-type subcollector can be embedded in the N-epi layer (see Page 2, paragraph [0020] of Chen).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Coolbaugh reference with the p-type semiconductor layer formed beneath the n-type subcollector as taught by Chen in order for the N-epi layer to be formed thereon so that the n-type subcollector can be embedded in the N-epi layer (see Page 2, paragraph [0020] of Chen).

In re claim 12, as applied to claim 9 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the upper region of the semiconductor substrate **10** comprises an epitaxial semiconductor layer (optional epi Si layer, not shown) (see page 2, paragraph [0039] of Coolbaugh).

In re claim 13, as applied to claim 9 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein field effect transistor further comprises a gate dielectric **52** located beneath the gate conductor **54**, a hard mask **56** located on the gate conductor **54**, at least one spacer located on sidewalls of the gate conductor **54** and abutting source/drain regions (see page 3, paragraph [0059] to page 4, paragraph [0050] and FIG. 9 of Coolbaugh).

In re claim 14, as applied to claim 9 above, Coolbaugh in combination with Chen discloses all claimed limitations including the limitation wherein the gate conductor **54** comprises polysilicon (see page 3, paragraph [0049] of Coolbaugh).

Response to Applicants' Amendment and Arguments

4. Applicants' arguments with respect to claims 1-3, 6-9 and 12-14 have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendment filed on August 25th, 2008.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kiem D. Nguyen/
Examiner, Art Unit 2823

/K. D. N./
January 15th, 2009